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PATENT ABSTRACTS OF JAPAN

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(71)Applicant : CASIO COMPUT CO LTD

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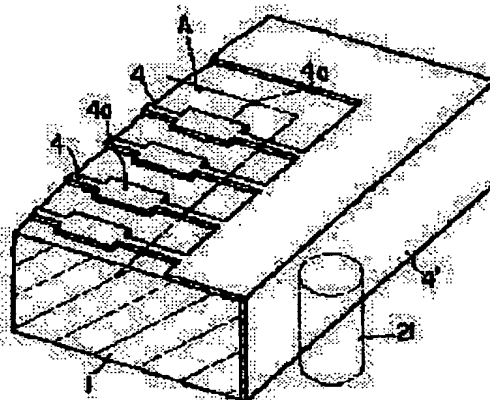
(72)Inventor : YOSHINO MASAO

(54) PRODUCTION OF THIN-FILM TRANSISTOR PANEL

(57)Abstract:

PURPOSE: To improve the yield of production by preventing the dielectric breakdown and degradation in performance of thin-film transistors(TFTs) by influence of static electricity.

CONSTITUTION: A conductive thin film is formed uniformly over the entire surface of the front surface of a transparent substrate 1 and the side faces thereof. The thin film is etched to form plural gate lines 4 to be arranged within the prescribed region A on the substrate 1 and a conductive parts 4' which are arranged from the outer side of the region A of the substrate 1 to the side faces of the substrate 1 and conduct electrically to the respective gate lines 4. The substrate 1 is arranged on a metallic rubbing stage to electrically conduct the respective gate lines 4 via the conductive parts 4' to the rubbing stage and the surfaces of oriented films are rubbed in this state at the time of forming the TFTs, pixel electrodes, data lines and oriented films on the region A and subjecting the surfaces of the oriented film to a rubbing treatment. The substrate 1 is scribed along the contours of the region A after the rubbing treatment, by which the conductive parts 4' are removed and the respective gate lines 4 are made independent.



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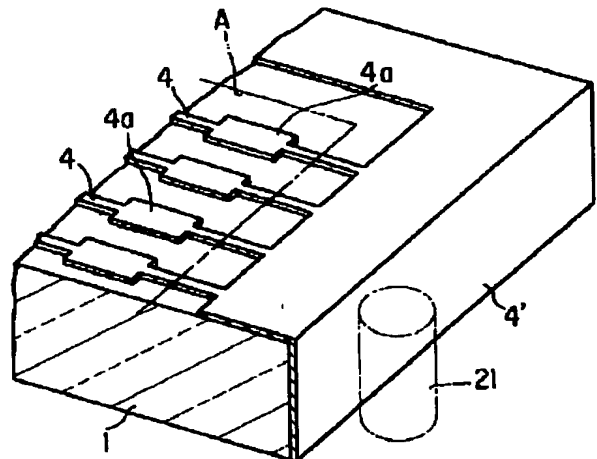
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(54) 【発明の名称】 薄膜トランジスタパネルの製造方法

(57) 【要約】

【目的】 静電気の影響による薄膜トランジスタの絶縁破壊や性能低下を防止して製造の歩留りを向上させる。

【構成】 透明な基板1の上面の全体およびその側面に亘って一様に導電性の薄膜を形成し、この薄膜をエッチングして、基板1の上の所定の領域A内に配置する複数のゲートライン4と、基板1の前記領域Aの外側から基板1の側面に亘って配置しかつ前記各ゲートライン4に電気的に導通する導電部4'とを形成し、領域Aの上に薄膜トランジスタ2、画素電極3、データライン5および配向膜17を形成し、配向膜17の膜面にラビング処理を施す際に、基板1を金属製のラビングステージ20の上に配置し、各ゲートライン4を導電部4'を介してラビングステージ20に電気的に導通させ、この状態で配向膜17の膜面をラビングし、このラビングの処理後に、基板1を領域Aの輪郭に沿ってスクライブすることにより導電部4'を除去して各ゲートライン4を独立させる。



【特許請求の範囲】

【請求項 1】 透明な基板の上に、複数の薄膜トランジスタと、これら薄膜トランジスタに接続する複数の画素電極と、前記薄膜トランジスタにゲート信号を供給する複数のゲートラインと、前記薄膜トランジスタにデータ信号を供給する複数のデータラインとが形成され、さらに前記基板の上に配向膜が形成され、この配向膜の膜面にラビング処理が施されている薄膜トランジスタパネルを製造する方法であって、

透明な基板の上面の全体およびその側面に亘って一様に導電性の薄膜を形成し、この薄膜をフォトリソグラフィによりエッチングして、基板の上の所定の領域内に配置する複数のゲートラインと、基板の前記領域の外側から基板の側面に亘って配置しかつ前記各ゲートラインに電気的に導通する導電部とをパターン形成し、前記領域の上に薄膜トランジスタ、画素電極、データラインおよび配向膜を形成し、前記配向膜の膜面にラビング処理を施す際に、前記基板を金属製のラビングステージの上に配置し、前記各ゲートラインを前記導電部を介して前記ラビングステージに電気的に導通させ、この状態で配向膜の膜面をラビングし、このラビングの処理後に、基板を前記領域の輪郭に沿ってスクライブすることにより前記導電部を除去して各ゲートラインを独立させることを特徴とする薄膜トランジスタパネルの製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 本発明は、アクティブマトリックス型の液晶表示素子に用いられる薄膜トランジスタパネルの製造方法に関する。

【0002】

【従来の技術】 アクティブマトリックス型の液晶表示素子は、薄膜トランジスタパネルと対向パネルとを、枠状のシール材を介して接合し、この両パネル間の前記シール材で囲まれた領域内に液晶を封入してなる。

【0003】 薄膜トランジスタパネルは、ガラス等からなる透明な基板の上に、縦横に配列する複数の薄膜トランジスタと、これら薄膜トランジスタに接続する複数の透明な画素電極と、前記薄膜トランジスタにゲート信号を供給する複数のゲートラインと、前記薄膜トランジスタにデータ信号を供給する複数のデータラインとを形成し、さらに基板の上に前記各画素電極および各薄膜トランジスタを覆うポリイミド等からなる配向膜を塗布し、この配向膜の膜面にラビング処理を施してなる。

【0004】 そしてこのように構成された薄膜トランジスタパネルが液晶表示素子の組立工程に送られ、この薄膜トランジスタパネルと対向パネルとが、枠状のシール材を介して接合されて液晶表示素子が組み立てられる。

【0005】

【発明が解決しようとする課題】 ところが、薄膜トランジスタパネルの製造工程時に配向膜の膜面にラビング

処理を施すと、ラビング布と配向膜との摩擦で静電気が発生して基板の表面が帯電し、この帯電で薄膜トランジスタに絶縁破壊や性能低下が発生してしまうことがある。

【0006】 本発明はこのような点に着目してなされたもので、その目的とするところは、静電気の影響による薄膜トランジスタの絶縁破壊や性能低下を防止して製造の歩留りを向上させることができる薄膜トランジスタパネルの製造方法を提供することにある。

【0007】

【課題を解決するための手段】 本発明はこのような目的を達成するために、透明な基板の上に、複数の薄膜トランジスタと、これら薄膜トランジスタに接続する複数の画素電極と、前記薄膜トランジスタにゲート信号を供給する複数のゲートラインと、前記薄膜トランジスタにデータ信号を供給する複数のデータラインとが形成され、さらに前記基板の上に配向膜が形成され、この配向膜の膜面にラビング処理が施されている薄膜トランジスタパネルを製造する方法であって、透明な基板の上面の全体およびその側面に亘って一様に導電性の薄膜を形成し、この薄膜をフォトリソグラフィによりエッチングして、基板の上の所定の領域内に配置する複数のゲートラインと、基板の前記領域の外側から基板の側面に亘って配置しかつ前記各ゲートラインに電気的に導通する導電部とをパターン形成し、前記領域の上に薄膜トランジスタ、画素電極、データラインおよび配向膜を形成し、前記配向膜の膜面にラビング処理を施す際に、前記基板を金属製のラビングステージの上に配置し、前記各ゲートラインを前記導電部を介して前記ラビングステージに電気的に導通させ、この状態で配向膜の膜面をラビングし、このラビングの処理後に、基板を前記領域の輪郭に沿ってスクライブすることにより前記導電部を除去して各ゲートラインを独立させるようにしたものである。

【0008】

【作用】 配向膜のラビング処理時には、配向膜の膜面とラビング布との摩擦により静電気が発生して基板の表面に静電気が帯電しようとするが、基板にはゲートラインのパターニング時にそのゲートラインと一体に形成された導電部が残っており、この導電部が基板の上面から側面に亘って配置してラビングステージに電気的に導通しており、このためラビング処理時に静電気が発生しても、この静電気が前記導電部を通してラビングステージにアースされ、したがって基板の表面での帯電が防止され、薄膜トランジスタの絶縁破壊や性能低下の発生が避けられる。

【0009】

【実施例】 以下、本発明の一実施例について図面を参照して説明する。一般に液晶表示素子は、その複数個を一括して組み立てる製法で製造されており、この製法で液晶表示素子を製造する場合は、一枚の大型基板を用いて

の側面に亘って配置しかつ前記各ゲートライン4に電氣的に導通する導電部4'とをパターン形成する。

【0017】次に、各領域Aの上に、薄膜トランジスタ2、画素電極3、データライン5および配向膜17を形成する。この後、大型基板1を、図5に示すように金属製のラビングステージ20の上に配置し、そのラビングステージ20の上面に突設されている金属製の位置決めピン21に大型基板1の側面を図1に示すように当てて大型基板1をラビングステージ20の上の所定の位置に定置させる。

【0018】この状態で前記配向膜17の膜面に、ナイロン、レーヨン、綿等のラビング布を巻き付けたラビングローラ22を接触させ、このラビングローラ22を回転させながら一方方向に移動させて配向膜17の膜面にラビング処理を施す。

【0019】このとき、配向膜17の膜面とラビングローラ22との摩擦により静電気が発生して大型基板1の表面に静電気が帯電しようとする。ところが、大型基板1の上面から側面に亘る部分には、ゲートライン4のパターニング時にそのゲートライン4と一体に形成された導電部4'が残っており、この導電部4'が基板1の側面において位置決めピン21に接触してラビングステージ20に電気的に導通しており、このためラビング処理時に静電気が発生しても、この静電気が前記導電部4'を通してラビングステージ20にアースされ、したがって基板1の表面が帯電することがなく、これにより薄膜トランジスタ2の絶縁破壊や性能低下の発生が防止される。

【0020】配向膜17の膜面に対するラビング処理後には、大型基板1を液晶表示素子の組立工程に送り、薄膜トランジスタパネルと対向パネルとを枠状のシール材により接合して液晶表示素子を組み立てる。

【0021】液晶表示素子の組み立て後には、薄膜トランジスタパネルの大型基板1および対向パネルの大型基板をそれぞれスクライブして液晶表示素子の個々を分離させる。この分離の際に、薄膜トランジスタパネルの大型基板1においては、前記領域Aの輪郭に沿ってスクライブし、領域Aの外側を除去する。領域Aの外側には導電部4'が配置しており、したがってスクライブにより領域Aの外側が除去されることにより、前記導電部4'も同時に除去され、この除去により領域Aの上に配置する各ゲートライン4がそれぞれ独立し、最終的な薄膜トランジスタパネルとしての構成が整う。

【0022】なお、本発明は、大型基板を用いて複数の薄膜トランジスタパネルを一括して形成する場合に限らず、薄膜トランジスタパネル一個分の採取が可能な大きさの基板を用いて薄膜トランジスタパネルを製造する場合であってもよい。

【0023】
【発明の効果】以上説明したように本発明によれば、配

5

向膜の膜面のラビング処理時に静電気が発生してもその静電気をラビングステージにアースさせて基板の表面における帯電を防止でき、したがってその帯電に起因する薄膜トランジスタの絶縁破壊や性能低下を防止して歩留りのよい製造を達成することができる。

【図面の簡単な説明】

【図1】本発明の一実施例を示す薄膜トランジスタパネルの一部の斜視図。

【図2】複数の薄膜トランジスタの採取が可能な大きさに形成された大型基板の斜視図。

【図3】薄膜トランジスタパネルの一部の平面図。

【図4】薄膜トランジスタの構造を示す断面図。

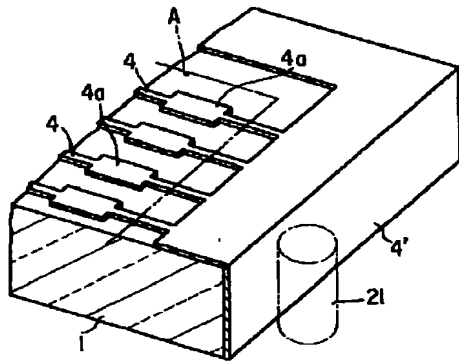
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【図5】薄膜トランジスタパネルの配向膜にラビング処理を施すときの状態を示す側面図。

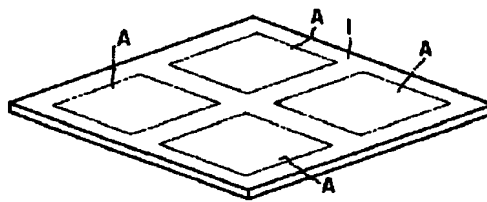
【符号の説明】

- 1…基板
- 2…薄膜トランジスタ
- 3…画素電極
- 4…ゲートライン
- 4'…導電部
- 5…データライン
- 10 17…配向膜
- 20…ラビングステージ

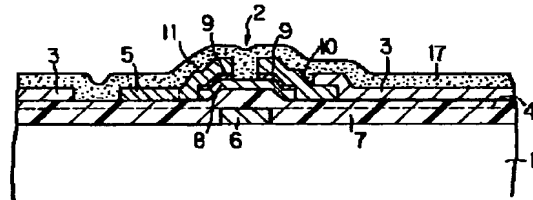
【図1】



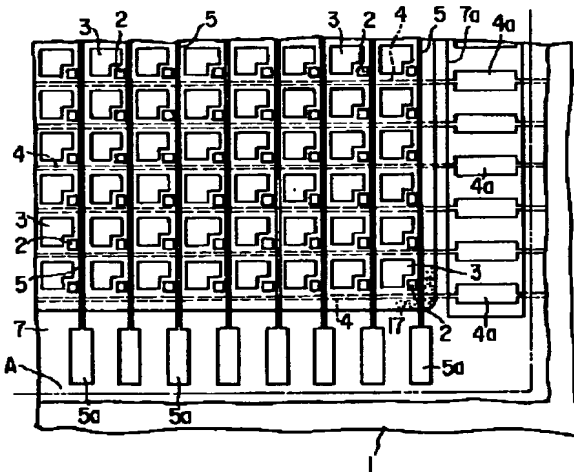
【図2】



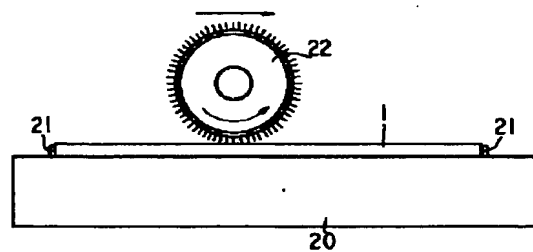
【図4】



【図3】



【図5】



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CLAIMS

[Claim(s)]

[Claim 1] Two or more pixel electrodes which connect with two or more TFT and these TFT on a transparent substrate, Two or more gate lines which supply a gate signal to the aforementioned TFT, Two or more data lines which supply a data signal to the aforementioned TFT are formed. It is the method of manufacturing the TFT panel by which an orientation film is furthermore formed on the aforementioned substrate, and rubbing processing is performed to the film surface of this orientation film. Form a conductive thin film uniformly covering the whole upper surface of a transparent substrate, and its side, and this thin film is *****ed by the photolithography. Arrange covering the side of a substrate from two or more gate lines arranged in a field predetermined [on a substrate], and the outside of the aforementioned field of a substrate, and pattern formation of the current carrying part through which it flows electrically is carried out to each aforementioned gate line. TFT, a pixel electrode, a data line, and an orientation film are formed on the aforementioned field. In case rubbing processing is performed to the film surface of the aforementioned orientation film, the aforementioned substrate is arranged on a metal rubbing stage. The aforementioned rubbing stage is made to flow through each aforementioned gate line electrically through the aforementioned current carrying part. The manufacture method of the TFT panel characterized by removing the aforementioned current carrying part and making each gate line become independent by carrying out rubbing of the film surface of an orientation film in this state, and carrying out the scribe of the substrate along with the profile of the aforementioned field after processing of this rubbing.

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DETAILED DESCRIPTION

Detailed Description of the Invention]

0001]

Industrial Application] this invention relates to the manufacture method of the TFT panel used for an active matrix type liquid crystal display element.

0002]

Description of the Prior Art] An active matrix type liquid crystal display element joins a TFT panel and an opposite panel through a frame-like sealant, and comes to enclose liquid crystal in the field surrounded by the aforementioned sealant between both this panel.

0003] Two or more TFT arranged in all directions on the transparent substrate which a TFT panel becomes from glass etc., Two or more transparent pixel electrodes linked to these TFT, and two or more gate lines which supply a gate signal to the aforementioned TFT, Two or more data lines which supply a data signal to the aforementioned TFT are formed, the orientation film which consists each aforementioned pixel electrode and each TFT of a wrap polyimide etc. on a substrate further is applied, and it comes to give rubbing processing to the film surface of this orientation film.

0004] And the TFT panel constituted in this way is sent like the erector of a liquid crystal display element, this TFT panel and an opposite panel are joined through a frame-like sealant, and a liquid crystal display element is assembled.

0005]

Problem(s) to be Solved by the Invention] However, when rubbing processing is performed to the film surface of an orientation film at the time of the manufacturing process of TFT TAPANERU, static electricity occurs in friction with a rubbing cloth and an orientation film, the front face of a substrate may be charged and dielectric breakdown and degradation may occur in TFT in this electrification.

0006] this invention was made paying attention to such a point, and the place made into the purpose is to offer the manufacture method of the TFT panel which can prevent dielectric breakdown and degradation of TFT under the influence of static electricity, and can raise the yield of manufacture.

0007]

Means for Solving the Problem] The TFT of plurality [top / substrate / transparent in order that this invention may attain such a purpose], Two or more pixel electrodes linked to these TFT, and two or more gate lines which supply a gate signal to the aforementioned TFT, Two or more data lines which supply a data signal to the aforementioned TFT are formed. It is the method of manufacturing the TFT panel by which an orientation film is furthermore formed on the aforementioned substrate, and rubbing processing is performed to the film surface of this orientation film. Form a conductive thin film uniformly covering the whole upper surface of a transparent substrate, and its side, and this thin film is *****ed by the photolithography. Arrange covering the side of a substrate from two or more gate lines arranged in a field predetermined [on a substrate], and the outside of the aforementioned field of a substrate, and pattern formation of the current carrying part through which it flows electrically is carried out to each aforementioned gate line. TFT, a pixel electrode, a data line, and an orientation film are formed on the aforementioned field. In case rubbing processing is performed to the film surface of the aforementioned orientation film, the aforementioned substrate is arranged on a metal rubbing stage. The aforementioned rubbing stage is made to flow through each aforementioned gate line electrically through the aforementioned current carrying part. The aforementioned current carrying part is removed and it is made to make each gate line become independent by carrying out rubbing of the film surface of an orientation film in this state, and carrying out the scribe of the substrate along with the profile of the aforementioned field after processing of this rubbing.

0008]

Function] Although static electricity tends to occur by friction with the film surface of an orientation film, and a rubbing cloth and it is going to charge static electricity on the surface of a substrate at the time of rubbing processing of

an orientation film The current carrying part formed in the gate line and one at the time of patterning of a gate line remains in the substrate. Even if this current carrying part has arranged ranging from the upper surface to the side of a substrate, it has flowed electrically on the rubbing stage and static electricity occurs at the time of rubbing processing for this reason This static electricity is grounded to a rubbing stage through the aforementioned current carrying part, therefore electrification in the front face of a substrate is prevented, and dielectric breakdown of TFT and generating of degradation are avoided.

[0009]

[Example] Hereafter, one example of this invention is explained with reference to a drawing. When it is manufactured by the process which assembles the plurality collectively and manufactures a liquid crystal display element by this process, after a liquid crystal display element constitutes the TFT panel for liquid crystal display element plurality using one large-sized substrate and assembles it as a liquid crystal display element, it carries out the scribe of the aforementioned large-sized substrate for every portion of each TFT panel, and it is made to separate it generally.

[0010] The transparent large-sized substrate 1 which becomes drawing 2 from the glass formed in the size which can extract the TFT panel for liquid crystal display element plurality is shown, on this substrate 1, four predetermined fields A are secured and the TFT panel is constituted in each of that field A.

[0011] That is, in each field A on a substrate 1, as shown in drawing 3, two or more TFT 2 arranged in all directions, two or more transparent pixel electrodes 3 linked to these TFT 2, two or more gate lines 4 which supply a gate signal to aforementioned TFT 2, and two or more data lines 5 which supply a data signal to aforementioned TFT 3 are formed.

[0012] The gate line 4 which wired on the substrate 1 as aforementioned TFT 2 was shown in drawing 4, and the gate electrode 6 formed in one, The gate insulator layer 7 which consists this gate electrode 6 of a wrap SiN (silicon nitride) etc., The i-type-semiconductor film 8 which consists of a-Si (amorphous silicon) which was made to counter the aforementioned gate electrode 6 and was formed on this gate insulator layer 7, It consists of the source electrodes 10 and the drain electrodes 11 which were formed through the n-type-semiconductor film 9 which consists of a-Si which doped the impurity on this i-type-semiconductor film 8.

[0013] The aforementioned gate insulator layer 7 covers the aforementioned gate line 4, and is formed all over the simultaneously in Field A, and the aforementioned pixel electrode 3 and the data line 5 are formed on the aforementioned gate insulator layer 7. And the pixel electrode 3 is connected to the source electrode 10 of TFT 2 in the end edge, and the data line 5 is connected with the drain electrode 11 of TFT 2 in one.

[0014] In addition, in drawing 3, the terminal with which 4a was formed in the end section of the gate line 4, and 5a are the terminals formed in the end section of a data line 5, and terminal 4a of the gate line 4 is exposed by forming opening 7a in the aforementioned gate insulator layer 7, after forming a data line 5.

[0015] Furthermore, on each field A, the orientation film 17 which consists of a polyimide etc. is formed so that TFT 2 and the pixel electrode 3 may be covered, and rubbing processing is performed to the film surface of this orientation film 17.

[0016] When the process which manufactures this TFT panel is explained, the conductive thin film by aluminum system alloy etc. is made to adhere uniformly first covering the whole upper surface of the large-sized substrate 1, and its side by the sputter or the vacuum deposition. And as it *****s by the photolithography and the aforementioned thin film is shown in drawing 1, it arranges covering the side of a substrate 1 from the gate line 4 arranged on each field A of a substrate 1, and the outside of Field A, and pattern formation of current-carrying-part 4' through which it flows electrically is carried out to each aforementioned gate line 4.

[0017] Next, TFT 2, the pixel electrode 3, a data line 5, and the orientation film 17 are formed on each field A. Then, the large-sized substrate 1 is arranged on the metal rubbing stage 20, as shown in drawing 5, the side of the large-sized substrate 1 is applied to the metal gage pin 21 which protrudes on the upper surface of the rubbing stage 20, as shown in drawing 1, and the position on the rubbing stage 20 is made to fix the large-sized substrate 1.

[0018] Contacting the rubbing roller 22 which twisted rubbing cloths, such as nylon, rayon, and cotton, to the film surface of the aforementioned orientation film 17, and making it rotate this rubbing roller 22 in this state, on the other hand, it is made to move to **, and rubbing processing is performed to the film surface of the orientation film 17.

[0019] At this time, static electricity tends to occur by friction with the film surface of the orientation film 17, and the rubbing roller 22, and it is going to charge static electricity on the front face of the large-sized substrate 1. however, into the portion ranging from the upper surface to the side of the large-sized substrate 1 Current-carrying-part 4' formed in the gate line 4 and one at the time of patterning of the gate line 4 remains. Even if this current-carrying-part 4' contacted the gage pin 21 in the side of a substrate 1, it has flowed electrically on the rubbing stage 20 and static electricity occurs at the time of rubbing processing for this reason This static electricity is grounded to the rubbing stage 20 through aforementioned current-carrying-part 4', therefore the front face of a substrate 1 is not charged, and, thereby, dielectric breakdown of TFT 2 and generating of degradation are prevented.

[0020] After the rubbing processing to the film surface of the orientation film 17, the large-sized substrate 1 is sent like the erector of a liquid crystal display element, a TFT panel and an opposite panel are joined by the frame-like sealant, and a liquid crystal display element is assembled.

[0021] The scribe of the large-sized substrate 1 of a TFT panel and the large-sized substrate of an opposite panel is carried out, respectively, and each of a liquid crystal display element is made to separate after the assembly of a liquid crystal display element. In the case of this separation, in the large-sized substrate 1 of a TFT panel, a scribe is carried out along with the profile of the aforementioned field A, and the outside of Field A is removed. When current-carrying-part 4' arranges in the outside of Field A, therefore the outside of Field A is removed by the scribe, aforementioned current-carrying-part 4' is also removed simultaneously, each gate line 4 arranged on Field A by this removal becomes independent, respectively, and the composition as a final TFT panel is ready.

[0022] In addition, this invention may be the case where a TFT panel is manufactured using the substrate of the size in which not only when forming two or more TFT panels collectively using a large-sized substrate, but the extraction for a TFT panel piece is possible.

[0023]

[Effect of the Invention] Dielectric breakdown and degradation of TFT which are made to ground the static electricity to a rubbing stage, can prevent electrification in the front face of a substrate even if static electricity occurs at the time of rubbing processing of the film surface of an orientation film according to this invention as explained above, therefore originate in the electrification can be prevented, and good manufacture of the yield can be attained.

[Translation done.]

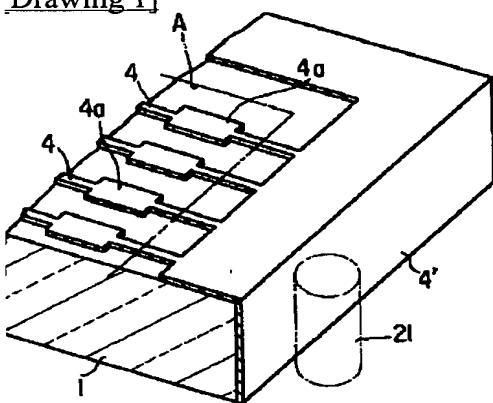
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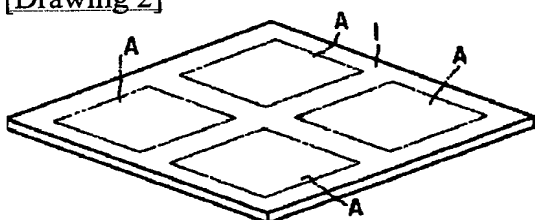
1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DRAWINGS

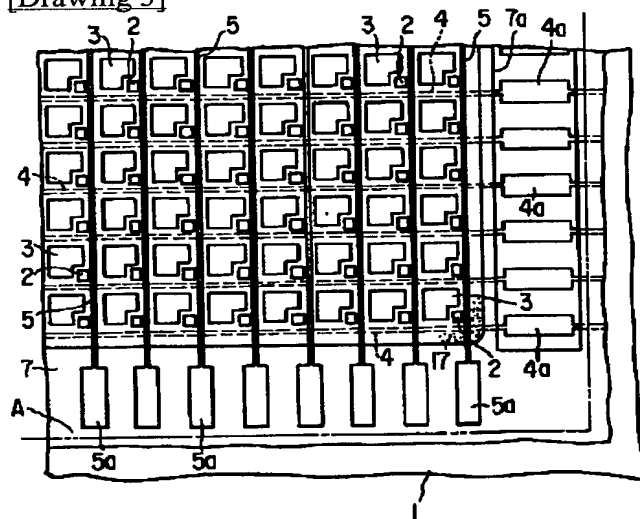
[Drawing 1]



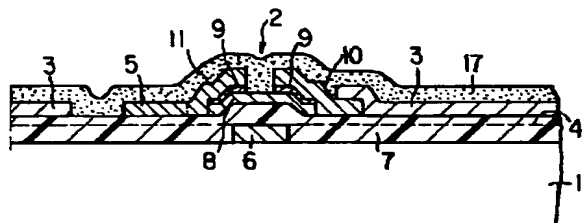
[Drawing 2]



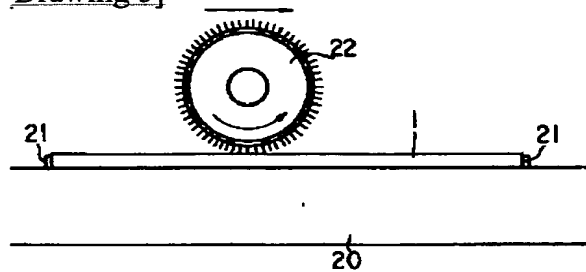
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]